

CDA 3201 Introduction to Logic Design Fall 2005

Dr. Hari Kalva

Science and Engineering Bldg. Rm. 422

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Classes: 10 – 11:50 am, Mon and Wed

Office Hours: MW: 11:50 – 1:00 pm,
or by appointment.

Goal: To develop an understanding of digital logic in order to analyze and design simple systems

Objectives:

- To provide fundamental proficiency in logic design
- Be able to simplify Boolean expressions using Boolean Algebra and K-map
- Be able to design small combinational and sequential circuits
- To understand basic techniques (such as algebraic manipulation) to accommodate design requirements
- Be able to build and test simple combinational and sequential circuits using IC chips.

Textbook: Introduction to Logic Design, Alan Marcovitz, Second Edition, McGraw-Hill, 2005.

Text website: http://higher.ed.mcgraw-hill.com/sites/0072865164/student_view0/

Course Grading:

Laboratory: 20 %

5 tests (5x10): 50%

Final exam (comprehensive): 30% (Sunday, December 4, 4:00 - 6:30 PM - TBD)

Topics:

- | | |
|------------------------------------|--|
| 1. Number Systems | 5. Solving Larger Combinational Problems |
| 2. Basics of Combinational Systems | 6. Sequential Systems |
| 3. Switching Algebra | 7. Solving Larger Sequential Problems |
| 4. The Karnaugh Map | 8. Simplification of Sequential Circuits |

Laboratory (S&E 324): You will design and build simple digital circuits based on the material covered in the class. For the laboratory experiments, you need a breadboard (to wire chips for the hardware experiments) which is available at the bookstore and the WinBreadboard software that comes with the textbook. You can also buy the breadboard from Radio Shack¹. **Read and follow the Lab Rules.** Have the lab instructor record grades on the Student Grading Sheet and turn that in at the Final Exam. Both the Lab Rules and the Student Grading Sheet are available through Blackboard. Details on obtaining lab accounts and 24-hour card-access to the lab will be provided later. **Lab opens on Wednesday, September 8.** Lab manual and grading sheet will be available from: <http://www.cse.fau.edu/~mplab/>.

Blackboard (blackboard.fau.edu): We will use Blackboard for course related announcements, handouts, reporting grades etc. You can login to blackboard at: blackboard.fau.edu. We will use e-mail for all announcements; make sure you update your e-mail address in the Blackboard and check your e-mail often. Contact me with any login problems.

Course Policies:

1. Each student is required to do his or her own work. Collaborative work may be undertaken only when specifically requested or approved by the instructor. Any academic irregularity (i.e. cheating) will not be tolerated and will result in a 0 on that assignment (with a minimum reduction of one letter grade in the course) and possibly an F in this course.
2. No 'I' grades or make up tests except in extreme and documented circumstances beyond your control.
3. Late labs up to a whole week are graded with 50% off, and after a week you get 0.

Cell phones must be turned off or in silent mode during the class!

¹ RadioShack 6" Modular IC Breadboard Socket, Catalog #: 276-174 Model: 276-174 , \$14.99

CDA 3201 Logic Design -- MW, 10:00 to 11:50 am, GS 103

8/22/2005	
8/24/2005	
8/29/2005	Last day to add/drop
8/31/2005	
9/5/2005	Labor day holiday
9/6/2005	Lab Opens
9/7/2005	Test 1; Lab Opens
9/12/2005	
9/14/2005	
9/19/2005	
9/21/2005	
9/23/2005	Lab 1 and Lab 2 due
9/26/2005	Test 2
9/28/2005	
10/3/2005	
10/5/2005	
10/7/2005	Lab 3 due
10/10/2005	
10/12/2005	Test 3, Design Project Assignment
10/14/2005	Last day to withdraw
10/17/2005	
10/19/2005	E-mail project teams
10/21/2005	Lab 4 due
10/24/2005	
10/26/2005	
10/31/2005	Test 4
11/2/2005	Part 1 of the project due
11/4/2005	Lab 5 due
11/7/2005	
11/9/2005	
11/14/2005	
11/16/2005	Test 5
11/18/2005	Lab 6
11/21/2005	
11/23/2005	
11/28/2005	Final Project due
11/30/2005	Lab 7 and 8 due
12/4/2005	Final Exam: 4:00 - 6:30 PM

Lab Assignments

Lab opens: Tuesday, Sept 6 (See schedule on the lab door or download it from www.cse.fau/~mplab)

All experiments from the text, pages 598 - 607 (as modified below).

Those labeled "Hardware" (H) must be implemented using the chips, board (which you must purchase) and IDL 800 Logic Lab available in Room SE-324A. Chips and wires are available in SE-324. See pp. 583 - 587.

Those labeled WinBreadboard (WB) are to be implemented using the simulator, which is one of the tools included on the CD-ROM packaged with the book. See pp. 587 - 589.

The last two labs can be implemented either way.

			Due
Lab 1	Experiment 1b	WinBreadboard	September 23
Lab 2	Experiment 1a	Hardware	September 23
Lab 3	Experiment 3f	Hardware	October 7
Lab 4	Experiment 5	WinBreadboard	October 21
Lab 5	Experiment 9a	WinBreadboard	November 4
Lab 6	Construct the circuit of Exercise 8c (Chapter 6) and test it.	Hardware	November 18
Lab 7	Experiment 19b using JK flip flops	either	November 23
Lab 8	Experiment 21 iv	either	November 30

The last day lab is open: Wednesday, November 30